

U.S. Patent Application Serial No. 10/613,260
Reply to Office Action dated December 16, 2004

Amendments to the Claims:

This listing of claims will replace all prior versions and listing of claims in the application.

Claims 1-3 and 6 are amended.

Listing of Claims:

1. (Currently Amended) A device $[(1)]$ for measuring the supply current (I_{DDQ}) to an electronic device under test DUT $[(5)]$, which is powered by a supply voltage (V_{DUT}), said measuring device $[(1)]$ being placed in a supply line between said supply voltage and said device under test $[(5)]$, said measuring device comprising a current measuring unit CMU $[(6)]$, a current bypass unit or CBU $[(20)]$ in parallel to said CMU, said CBU comprising a power MOSFET $[(22)]$ in the path between said supply voltage (V_{DUT}) and said DUT $[(5)]$, said CBU further comprising means to receive a clock signal $[(50)]$, being a succession of high and low states, said CBU comprising two transistors ~~(23/24 or 31/32)~~ connected by a series connection $[(30)]$, which receive said clock signal $[(50)]$ at their gates or bases, the gate of said MOSFET being connected to said series connection $[(30)]$, wherein a connection $[(51)]$ is present between one terminal other than the gate or base of one of said transistors in series, and the source of said MOSFET $[(22)]$.
2. (Currently Amended) The device according to claim 1, wherein said two transistors are respectively a P-MOS transistor $[(23)]$ and an N-MOS transistor $[(24)]$.
3. (Currently Amended) The device according to claim 1, wherein said two transistors are bipolar transistors, respectively a PNP transistor $[(31)]$ and an NPN transistor $[(32)]$.

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4. (Previously Amended) The device according to claim 1, wherein said two transistors in series are arranged as an inverter.
5. (Previously Presented) The device according to claim 1, wherein said two transistors in series are arranged as a follower driver.
6. (Currently Amended) The device according to claim 1, further comprising a processing unit $[(2)]$, which is in connection with said current measuring unit $[(6)]$ and with an output device $[(8)]$, and which is able to acquire an I_{DDQ} measured value from the CMU $[(6)]$, wherein the processing unit is able to perform processing actions on said measurement.
7. (Original) The device according to claim 6, wherein said processing actions are chosen from the group consisting of:
 - subtracting a measured I_{DDQ} value from a reference value or vice versa,
 - comparing a measured I_{DDQ} value with a reference value and producing a pass/fail signal on the basis of the result of said comparison,
 - subtracting a measured I_{DDQ} value from a previously measured I_{DDQ} value or vice versa,
 - comparing a calculated value, resulting from subtracting a measured I_{DDQ} value from a previously measured I_{DDQ} value or vice versa, or from subtracting a measured I_{DDQ} value from a reference value or vice versa, with a reference value and producing a pass/fail signal on the basis of the result of said comparison.
- 8-13. (Canceled)
14. (Original) A device according to claim 1, wherein said device is separate from said device under test.
15. (Original) A device according to claim 1, wherein said device is incorporated into said device under test.
- 16-17. (Canceled)